CLAIMS

1. Trigger circuit with hysteresis using the semiconductor on insulator technology, characterised in that it comprises at least two CMOS inverter stages, each inverter stage being composed of a first branch comprising at least one P-channel junction field effect transistor (PFET) in series between a first power supply potential V_{DD} and an output node from the inverter stage, and a second branch comprising at least one N-channel junction field effect transistor (NFET) in series between the said output node from the inverter stage and a second power supply potential, the said transistors of each inverter stage having their grids connected together to receive an input signal, the input to each of the inverters directly or indirectly receiving the input signal of the said circuit, the output signal from the said circuit being obtained directly or indirectly by the output signal from one of the inverter stages, and in that the substrate potential of each transistor of at least one inverter stage called the controlled inverter stage, is dynamically controlled by a control signal output from the said circuit.

2. Circuit according to claim 1, characterised in that the control signals controlling the said substrate potentials for transistors PFET and NFET of at least one controlled inverter stage are signals determined by the states of the circuit located on the output side of the said controlled inverter stage.

3. Circuit according to the above claim, characterised in that the said signals determined by the

states of the circuit located on the output side of the said controlled inverter stage are output signals from inverter stages called control inverter stages, located on the output side of the said controlled inverter stage.

4. Circuit according to the above claim, characterised in that the said control inverter stages are separated from the said controlled inverter stage by an even number (or zero) of inverter stages.

5. Circuit according to one of claims 1 to 4, characterised in that the substrate potentials for complementary transistors PFET and NFET of at least one controlled inverter state are controlled by the same control signal.

6. Circuit according to one of claims 1 to 4, characterised in that the substrate potentials for PFET transistors of at least one controlled inverter stage are controlled by a first control signal and substrate potentials for NFET transistors complementary to the said PFET transistors are controlled by a second control signal.

7. Circuit according to one of claims 1 to 4, characterised in that the substrate potentials for PFET transistors of at least one controlled inverter stage and substrate potentials for NFET transistors complementary to the said PFET transistors are all controlled by different control signals.

8. Circuit according to one of claims 1 to 4, characterised in that the substrate potentials for transistors of at least one controlled inverter stage included in a group of at least one pair of complementary

PFET and NFET transistors are controlled by the same control signal.

9. Circuit according to one of the above claims, characterised in that the substrate potential of transistors of the first inverter stage is controlled.

10. Circuit according to one of the above claims, characterised in that it includes three inverter stages.

11. Circuit according to the above claim, characterised in that the first two inverter stages are chained such that the output signal from the first inverter is applied to the input to the second inverter.

12. Circuit according to the above claim, characterised in that the second and third inverter stages are chained such that the output signal from the second inverter is applied to the input of the third inverter.

13. Circuit according to one of the above claims, characterised in that only the substrate potentials of transistors in the first stage are dynamically controlled, the substrate potentials for the transistors in inverter stages other than the first inverter stages not being controlled and being either left floating, or fixed to the power supply potentials of the circuit.

14. Circuit according to one of claims 1 to 12, characterised in that the substrate potentials for transistors in an inverter stage other than the last inverter stage are dynamically controlled by the output signal from the inverter stage located directly downstream on the output side, the substrate potentials for the transistors in the last inverter stage being either left

floating, or fixed to the power supply potentials of the circuit.

15. Circuit according to one of the above claims, characterised in that the trigger circuit with hysteresis is a Schmitt Trigger circuit.

16. Circuit according to one of the above claims, characterised in that it is used in the SOI technology.

17. Circuit integrated on a semiconductor on insulator substrate, characterised in that it comprises at least one trigger circuit with hysteresis according to one of the above claims.